40V Radiation Hardened and SET Enhanced Precision Low Power Operational Amplifier

ISL70219ASEH, ISL70419ASEH

The ISL70219ASEH and ISL70419ASEH are a family of very high precision amplifiers featuring the perfect combination of low noise vs power consumption. Low offset voltage, low I_{BIAS} current and low temperature drift making them the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of high precision, low noise, low power and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls and industrial controls.

The ISL70219ASEH is offered in a 10 lead hermetic ceramic flatpack. The ISL70419ASEH is offered in a 14 lead hermetic ceramic flatpack package. The devices are packaged in industry standard pin configurations and operate across the extended temperature range from -55°C to +125°C.

Related Literature

- UG007, "ISL70219ASEH Evaluation Board User Guide"
- TR002, "Single Event Effects (SEE) Testing of the ISL70219ASEH Dual Operational Amplifier"
- ISL70219ASEH SMD 5962-14226
- ISL70219ASEH Radiation Test Report

Features

- **Electrically screened to DLA SMD# 5962-14226**
- **Low input offset voltage. . . . . ±110µV, max**
- **Superb offset temperature coefficient. . . . . 1µV/°C, max**
- **Input bias current . . . . . ±15nA, max**
- **Input bias current TC . . . . . ±5pA/°C, max**
- **Low current consumption 440µA**
- Voltage noise . . . . . 8nV/√Hz
- Wide supply range . . . . . 4.5V to 36V
- Operating temperature range. . . . . -55°C to +125°C
- Radiation environment
  - SEB LET_{TH} (V_S = ±18V) . . . . . 86.4 MeV•cm^2/mg
  - SET recovery time . . . . . ≤10µs at 60 MeV•cm^2/m
  - SEL immune (SOI process)
  - Total dose HDR (50 to 300rad(Si)/s). . . . . 300krad(Si)
  - Total dose LDR (10mrad(Si)/s) . . . . . 100krad(Si) *

* Product capability established by initial characterization. The EH version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate.

Applications

- Precision instrumentation
- Spectral analysis equipment
- Active filter blocks, thermocouples and RTD reference buffers
- Data acquisition and power supply control

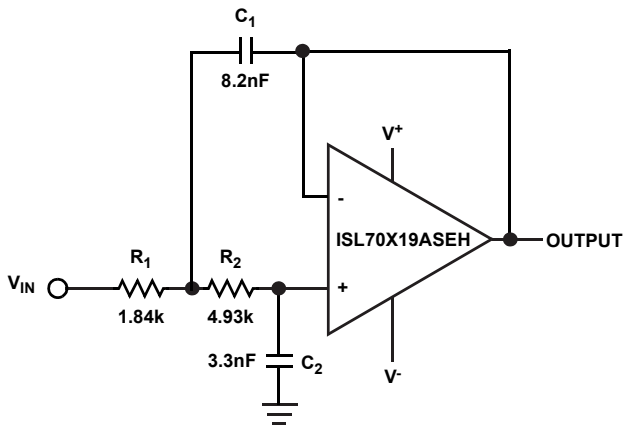


FIGURE 1. TYPICAL APPLICATION: SALLEN-KEY LOW PASS FILTER (F_C = 10kHz)

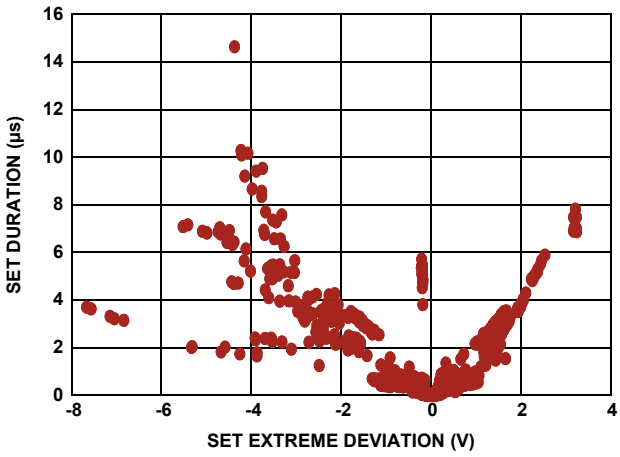
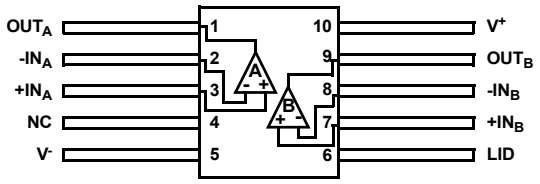


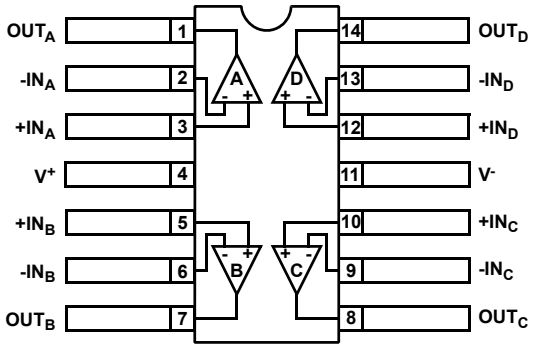
FIGURE 2. SET DEVIATION vs DURATION FOR LET = 60 MeV•cm^2/mg (V_S = ±18V)

Pin Configurations

ISL70219ASEH
(10 LD FLATPACK)
TOP VIEW

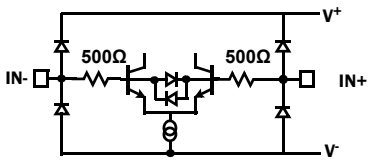


ISL70419ASEH6
(14 LD FLATPACK)
TOP VIEW

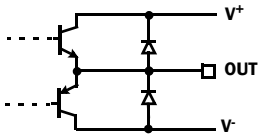


Pin Descriptions

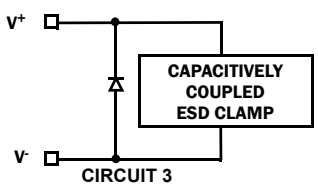
10 LD PIN NUMBER	14 LD PIN NUMBER	PIN NAME	EQUIVALENT ESD CIRCUIT	DESCRIPTION
1	1	OUT_A	Circuit 2	Amplifier A output
2	2	$-IN_A$	Circuit 1	Amplifier A inverting input
3	3	$+IN_A$	Circuit 1	Amplifier A noninverting input
10	4	V^+	Circuit 3	Positive power supply
7	5	$+IN_B$	Circuit 1	Amplifier B noninverting input
8	6	$-IN_B$	Circuit 1	Amplifier B inverting input
9	7	OUT_B	Circuit 2	Amplifier B output
-	8	OUT_C	Circuit 2	Amplifier C output
-	9	$-IN_C$	Circuit 1	Amplifier C inverting input
-	10	$+IN_C$	Circuit 1	Amplifier C noninverting input
5	11	V^-	Circuit 3	Negative power supply
-	12	$+IN_D$	Circuit 1	Amplifier D noninverting input
-	13	$-IN_D$	Circuit 1	Amplifier D inverting input
-	14	OUT_D	Circuit 2	Amplifier D output
-	E-Pad	E-Pad	None	E-Pad under package (unbiased, tied to package lid)
4	-	NC	-	No connect
6	-	LID	NA	Unbiased, tied to package lid



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Ordering Information

ORDERING/SMD NUMBER (Note 2)	PART NUMBER (Note 1)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F1422602VYC	ISL70219ASEHVF	-55 to +125	10 Ld Flatpack	K10.A
5962F1422602V9A	ISL70219ASEHVX	-55 to +125	Die	
ISL70219ASEHF/PROTO	ISL70219ASEHF/PROTO	-55 to +125	10 Ld Flatpack	K10.A
ISL70219ASEHF/SAMPLE	ISL70219ASEHVX/SAMPLE	-55 to +125	Die	
5962F1422603VXC (*Coming Soon*)	ISL70419ASEHVF	-55 to +125	14 Ld Flatpack	K14.C
5962F1422603V9A (*Coming Soon*)	ISL70419ASEHVX	-55 to +125	Die	
ISL70419ASEHF/PROTO (*Coming Soon*)	ISL70419ASEHF/PROTO	-55 to +125	14 Ld Flatpack	K14.C
ISL70419ASEHF/SAMPLE (*Coming Soon*)	ISL70419ASEHVX/SAMPLE	-55 to +125	Die	
ISL70219ASEHEV1Z	ISL70219ASEHEV1Z	Evaluation Board		
ISL70419ASEHEV1Z (Coming Soon)	ISL70419ASEHEV1Z	Evaluation Board		

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table must be used when ordering.

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Supply Voltage (Note 5). 36V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage 20V
Min/Max Input Voltage . . . . . V^- - 0.5V to V^+ + 0.5V
Max/Min Input Current for Input Voltage >V^+ or <V^- . . . . . ±20mA
Output Short-Circuit Duration (1 output at a time). . . . . Indefinite
ESD Rating
- Human Body Model (Tested per MIL-PRF-883 3015.7). 2kV
- Machine Model (Tested per EIA/JESD22-A115-A) 200V
- Charged Device Model (Tested per JESD22-C101D) 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld Flatpack Package (Notes 3, 4).	40	8
14 Ld Flatpack Package (Notes 3, 4).	35	8

Storage Temperature Range. . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Single Supply Voltage. . . . . 4.5V to 36.0V
Split Rail Supply Voltage . . . . . ±2.25V to ±18V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the package underside.
5. Tested in a heavy ion environment at LET = 86.4MeV • cm^2/mg at +125°C (T_C) for SEB. Refer to Single Event Effects Test Report for more information.

Electrical Specifications

V_S = ±18.0V, V_{CM} = V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted.
Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s, unless otherwise noted.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{OS}	Input Offset Voltage		-	10	85	µV
			-	-	**110**	µV
TCV_{OS}	Offset Voltage Drift	(Note 7)	**-**	0.1	**1**	µV/°C
I_B	Input Bias Current	T_A = +25°C	-2.5	0.08	2.5	nA
		T_A = -55°C, +125°C	**-5**	-	**5**	nA
		T_A = +25°C, post HDR/LDR Rad	**-15**	-	**15**	nA
TCI_B	Input Bias Current Temperature Coefficient	(Note 7)	**-5**	**1**	**5**	pA/°C
I_{OS}	Input Offset Current	T_A = +25°C	-2.5	0.08	2.5	nA
		T_A = -55°C, +125°C	**-3**	-	**3**	nA
		T_A = +25°C, post HDR/LDR Rad	**-10**	-	**10**	nA
TCI_{OS}	Input Offset Current Temperature Coefficient	(Note 7)	**-3**	**0.42**	**3**	pA/°C
V_{CM}	Input Voltage Range	Guaranteed by CMRR test	**-16**	-	**16**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = -16V to +16V	120	145	-	dB
			120	-	-	dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±20V	120	145	-	dB
			120	-	-	dB
A_{VOL}	Open-loop Gain	V_O = -16V to +16V, R_L = 10kΩ to ground	3,000	14,000	-	V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	16.5	16.7	-	V
			16.2	-	-	V
		R_L = 2kΩ to ground	16.3	16.5	-	V
			16.0	-	-	V

Electrical Specifications

V_S = ±18.0V, V_{CM} = V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s, unless otherwise noted. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground	-	-16.7	-16.5	V
			-	-	**-16.2**	V
		R_L = 2kΩ to ground	-	-16.5	-16.3	V
			-	-	**-16.0**	V
I_S	Supply Current/Amplifier		-	0.49	0.725	mA
			-	-	**0.85**	mA
I_{SC}	Output Short-circuit Current	Sourcing: V_{IN} = 0V, V_{OUT} = -16V (Note 7)	-	41	-	mA
		Sinking: V_{IN} = 0V, V_{OUT} = +16V (Note 7)	-	-42		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**±2.25**	-	**±20**	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, R_L = 2kΩ (Note 7)	-	1.5	-	MHz
e_{nVp-p}	Voltage Noise V_{P-P}	0.1Hz to 10Hz (Note 7)	-	0.25	-	μV_{P-P}
e_n	Voltage Noise Density	f = 10Hz (Note 7)	-	10	-	nV/√Hz
e_n	Voltage Noise Density	f = 100Hz (Note 7)	-	8.2	-	nV/√Hz
e_n	Voltage Noise Density	f = 1kHz (Note 7)	-	8	-	nV/√Hz
e_n	Voltage Noise Density	f = 10kHz (Note 7)	-	8	-	nV/√Hz
i_n	Current Noise Density	f = 1kHz (Note 7)	-	0.1	-	pA/√Hz
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	A_V = 1, R_L = 2kΩ, V_O = $4V_{P-P}$	0.3	0.5	-	V/µs
			0.2	-	-	V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}	-	130	450	ns
			-	-	**625**	ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = $50mV_{P-P}$, R_L = 10kΩ to V_{CM}	-	130	600	ns
			-	-	**700**	ns
t_s	Settling Time to 0.1% 10V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $10V_{P-P}$, R_L = 5kΩ to V_{CM} (Note 7)	-	21	-	µs
	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $10V_{P-P}$, R_L = 5kΩ to V_{CM} (Note 7)	-	24	-	µs
	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM} (Note 7)	-	13	-	µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = -1, V_{OUT} = $4V_{P-P}$, R_L = 5kΩ to V_{CM} (Note 7)	-	18	-	µs
t_{OL}	Output Positive Overload Recovery Time	A_V = -100, V_{IN} = $0.2V_{P-P}$, R_L = 2kΩ to V_{CM} (Note 7)	-	5.6	-	µs
	Output Negative Overload Recovery Time	A_V = -100, V_{IN} = $0.2V_{P-P}$, R_L = 2kΩ to V_{CM} (Note 7)	-	10.6	-	µs
OS+	Positive Overshoot	A_V = 1, V_{OUT} = $10V_{P-P}$, R_f = 0Ω R_L = 2kΩ to V_{CM}	-	15	-	%
			-	-	**33**	%
OS-	Negative Overshoot	A_V = 1, V_{OUT} = $10V_{P-P}$, R_f = 0Ω R_L = 2kΩ to V_{CM}	-	15	-	%
			-	-	**33**	%

Electrical Specifications

V_S = ±5.0V, V_{CM} = V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s, unless otherwise noted.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{OS}	Input Offset Voltage		-	10	150	µV
			-	-	**250**	µV
TCV_{OS}	Offset Voltage Drift	(Note 7)	**-**	0.1	**1**	µV/°C
I_B	Input Bias Current	T_A= +25°C	-2.5	0.08	2.5	nA
		T_A= -55°C, +125°C	**-5**	-	**5**	nA
		T_A= +25°C, post HDR/LDR Rad	**-15**	-	**15**	nA
TCI_B	Input Bias Current Temperature Coefficient	(Note 7)	**-5**	**1**	**5**	pA/°C
I_{OS}	Input Offset Current	T_A= +25°C	-2.5	0.3	2.5	nA
		T_A= -55°C, +125°C	**-3**	-	**3**	nA
		T_A= +25°C, post HDR/LDR Rad	**-10**	-	**10**	nA
TCI_{OS}	Input Offset Current Temperature Coefficient	(Note 7)	**-3**	**0.42**	**3**	pA/°C
V_{CM}	Input Voltage Range	Guaranteed by CMRR test	**-3**		**3**	V
CMRR	Common-mode Rejection Ratio	V_{CM} = -3V to +3V	120	145		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	120	145		dB
			120			dB
A_{VOL}	Open-loop Gain	V_O = -3.0V to +3.0V R_L = 10kΩ to ground	3,000	14,000		V/mV
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	3.5	3.7		V
			3.2			V
		R_L = 2kΩ to ground	3.3	3.55		V
			3.0			V
V_{OL}	Output Voltage Low	R_L = 10kΩ to ground		-3.7	-3.5	V
					-3.2	V
		R_L = 2kΩ to ground		-3.55	-3.3	V
					-3.0	V
I_S	Supply Current/Amplifier			0.47	0.675	mA
					0.8	mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 1k, R_L = 2kΩ (Note 7)		1.5		MHz
e_{nVp-p}	Voltage Noise V_{P-P}	0.1Hz to 10Hz (Note 7)	-	0.25	-	$µV_{P-P}$
e_n	Voltage Noise Density	f = 10Hz (Note 7)	-	12	-	nV/√Hz
e_n	Voltage Noise Density	f = 100Hz (Note 7)	-	8.6	-	nV/√Hz
e_n	Voltage Noise Density	f = 1kHz (Note 7)	-	8	-	nV/√Hz
e_n	Voltage Noise Density	f = 10kHz (Note 7)	-	8	-	nV/√Hz
i_n	Current Noise Density	f = 1kHz (Note 7)	-	0.1	-	pA/√Hz

Electrical Specifications $V_S = \pm5.0V$, $V_{CM} = V_O = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s, unless otherwise noted. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
TRANSIENT RESPONSE						
SR	Slew Rate, V_{OUT} 20% to 80%	$A_V = 1$, $R_L = 2k\Omega$, $V_O = 4V_{P-P}$ (Note 7)	-	0.5	-	V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM} (Note 7)	-	130	-	ns
	Fall Time 90% to 10% of V_{OUT}	$A_V = 1$, $V_{OUT} = 50mV_{P-P}$, $R_L = 10k\Omega$ to V_{CM} (Note 7)	-	130	-	ns
t_s	Settling Time to 0.1% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 5k\Omega$ to V_{CM} (Note 7)	-	12	-	µs
	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	$A_V = -1$, $V_{OUT} = 4V_{P-P}$, $R_L = 5k\Omega$ to V_{CM} (Note 7)	-	19	-	µs
t_{OL}	Output Positive Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$, $R_L = 2k\Omega$ to V_{CM} (Note 7)	-	7	-	µs
	Output Negative Overload Recovery Time	$A_V = -100$, $V_{IN} = 0.2V_{P-P}$, $R_L = 2k\Omega$ to V_{CM} (Note 7)	-	5.8	-	µs
OS+	Positive Overshoot	$A_V = 1$, $V_{OUT} = 10V_{P-P}$, $R_f = 0\Omega$ $R_L = 2k\Omega$ to V_{CM} (V)	-	15	-	%
OS-	Negative Overshoot	$A_V = 1$, $V_{OUT} = 10V_{P-P}$, $R_f = 0\Omega$ $R_L = 2k\Omega$ to V_{CM} (Note 7)	-	15	-	%

Electrical Specifications $V_S = \pm2.25V$, $V_{CM} = V_O = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s, unless otherwise noted.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{OS}	Input Offset Voltage			10	150	µV
					250	µV
TCV_{OS}	Offset Voltage Drift	(Note 7)		0.1	**1**	µV/°C
I_B	Input Bias Current	$T_A = +25°C$	-2.5	0.18	2.5	nA
		$T_A = -55°C, +125°C$	**-5**	-	**5**	nA
		$T_A = +25°C$, post HDR/LDR Rad	**-15**	-	**15**	nA
TCI_B	Input Bias Current Temperature Coefficient	(Note 7)	**-5**	**1**	**5**	pA/°C
I_{OS}	Input Offset Current	$T_A = +25°C$	-2.5	0.3	2.5	nA
		$T_A = -55°C, +125°C$	**-3**	-	**3**	nA
		$T_A = +25°C$, post HDR/LDR Rad	**-10**	-	**10**	nA
TCI_{OS}	Input Offset Current Temperature Coefficient	(Note 7)	**-3**	**0.42**	**3**	pA/°C
V_{CM}	Input Voltage Range	Guaranteed by CMRR Test	**-0.25**		**0.25**	V
CMRR	Common-mode Rejection Ratio	$V_{CM} = -0.25V$ to $+0.25V$	90	110		dB
			90			dB

Electrical Specifications

V_S = ±2.25V, V_{CM} = V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s, unless otherwise noted.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{OH}	Output Voltage High	R_L = 10kΩ to ground	0.8	1.03		V
			0.5			V
		R_L = 2kΩ to ground	0.75	0.98		V
			0.45			V
V_{OL}	Output Voltage High	R_L = 10kΩ to ground		-1.03	-0.8	V
					-0.5	V
		R_L = 2kΩ to ground		-0.98	-0.75	V
					-0.45	V

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. Guaranteed by characterization, not tested.

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C.

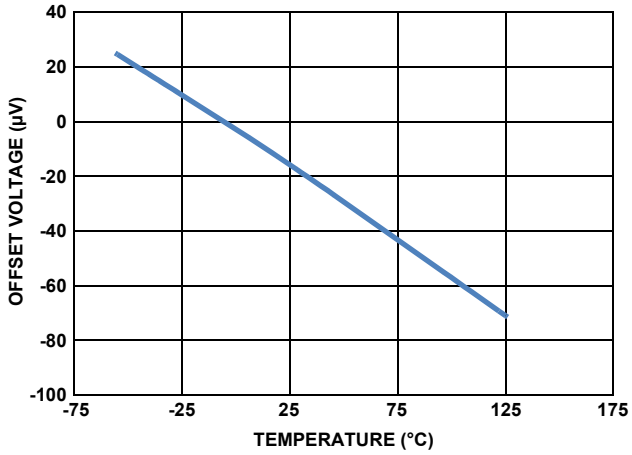


FIGURE 3. V_{OS} vs TEMPERATURE (±18V)

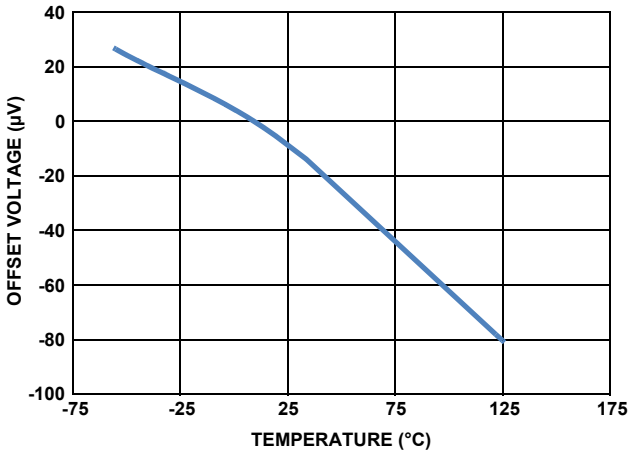


FIGURE 4. V_{OS} vs TEMPERATURE (±5V)

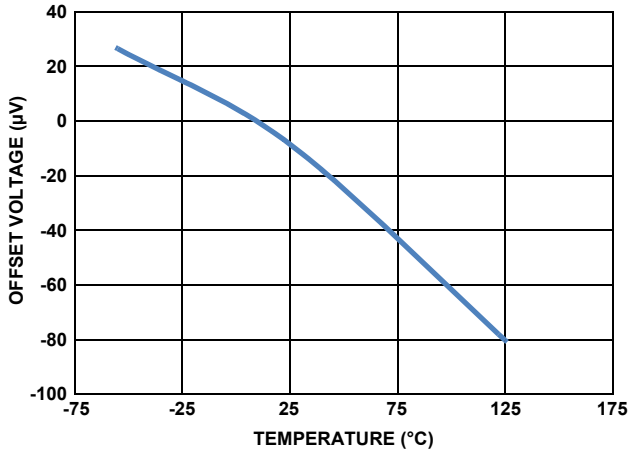


FIGURE 5. V_{OS} vs TEMPERATURE (±2.5V)

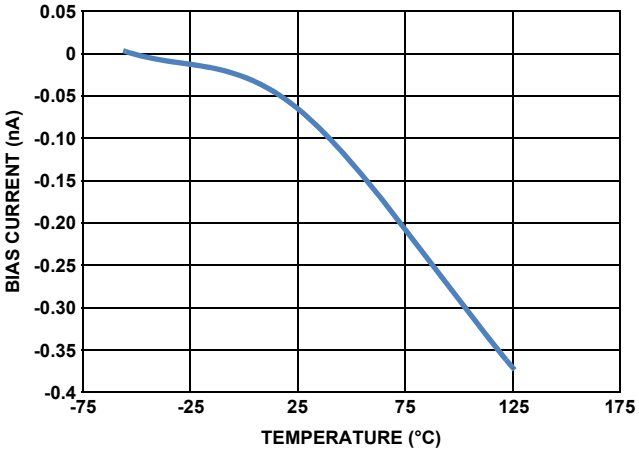


FIGURE 6. I_{BIAS} vs TEMPERATURE

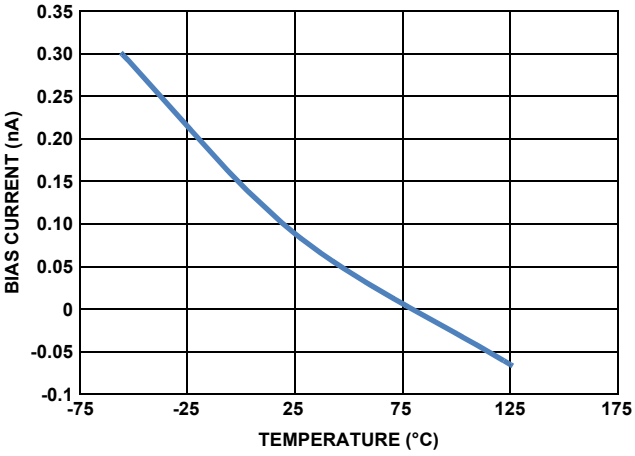


FIGURE 7. I_{BIAS} vs TEMPERATURE (±5V)

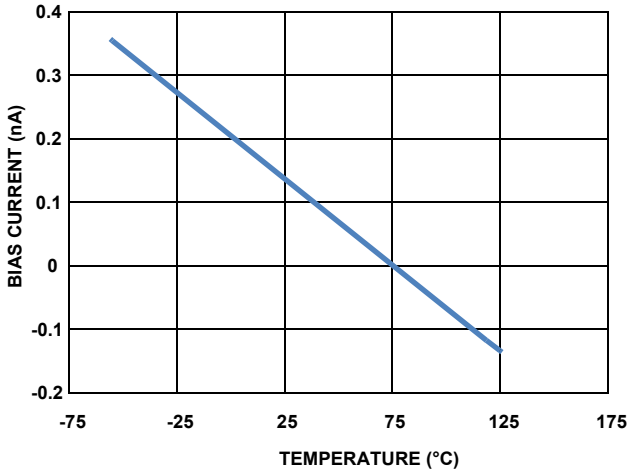


FIGURE 8. I_{BIAS} vs TEMPERATURE (±2.5V)

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

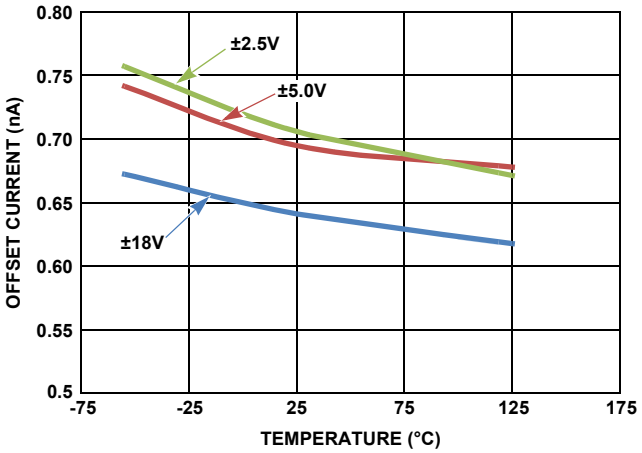


FIGURE 9. OFFSET CURRENT vs TEMPERATURE

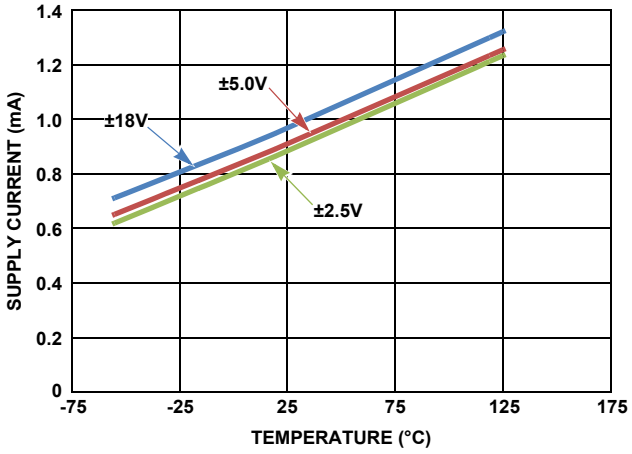


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

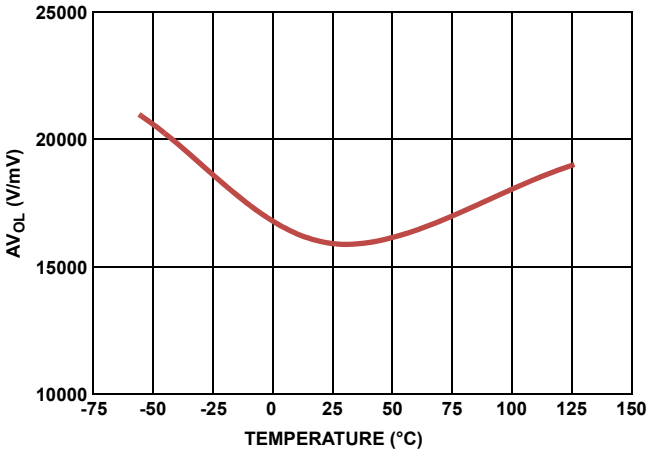


FIGURE 11. AV_{OL} vs TEMPERATURE (V_O = ±13V)

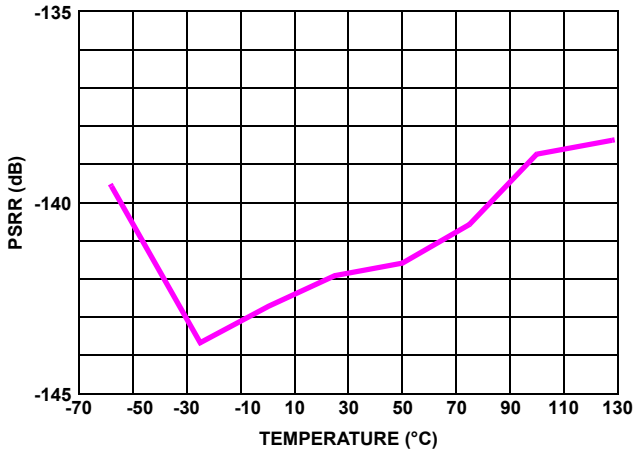


FIGURE 12. PSRR vs TEMPERATURE (±2.25V TO ±20V)

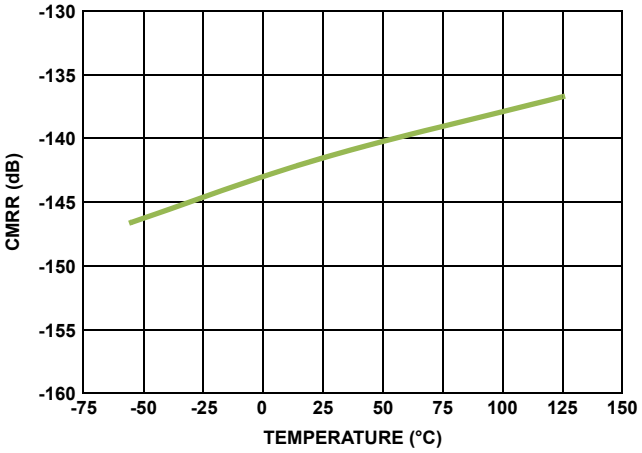


FIGURE 13. CMRR vs TEMPERATURE

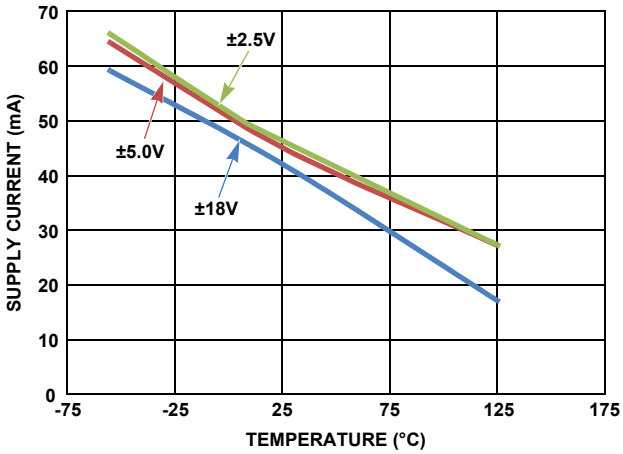


FIGURE 14. I_{SC} vs TEMPERATURE

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

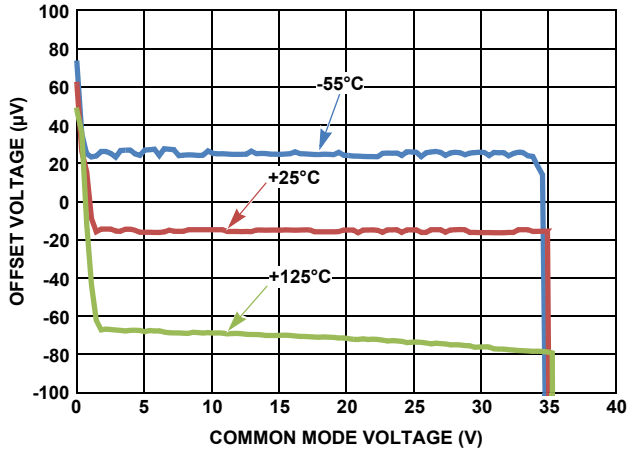


FIGURE 15. V_{OS} vs VCM (±18V)

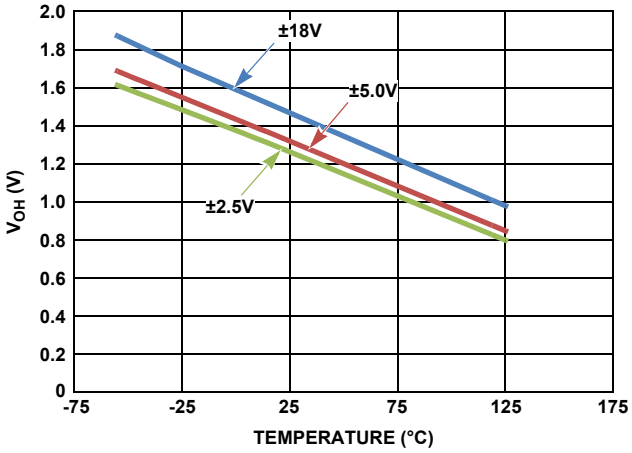


FIGURE 16. V_{OH} vs TEMPERATURE (R_L = 2k)

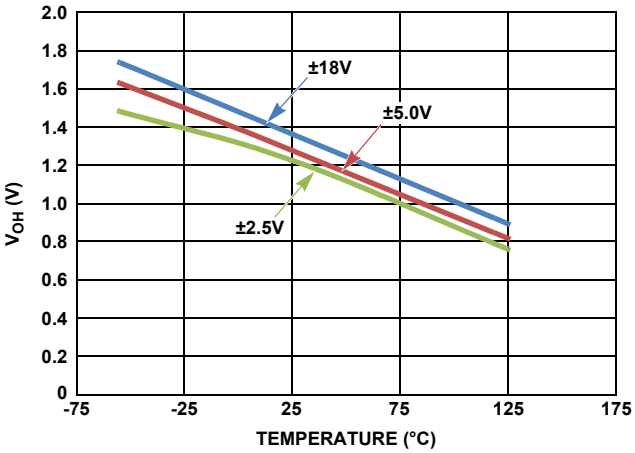


FIGURE 17. V_{OH} vs TEMPERATURE (R_L = 5k)

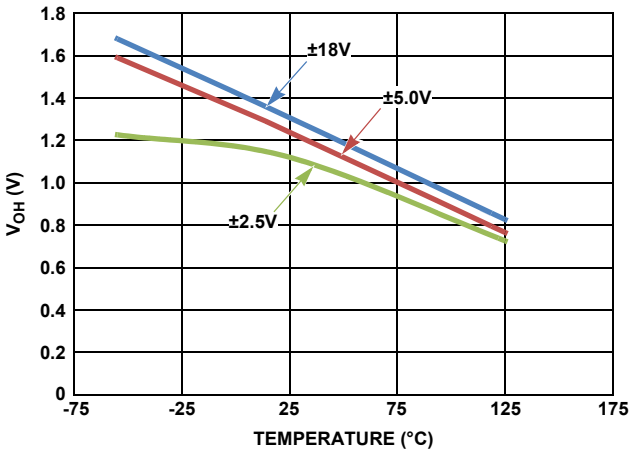


FIGURE 18. V_{OH} vs TEMPERATURE (R_L = 10k)

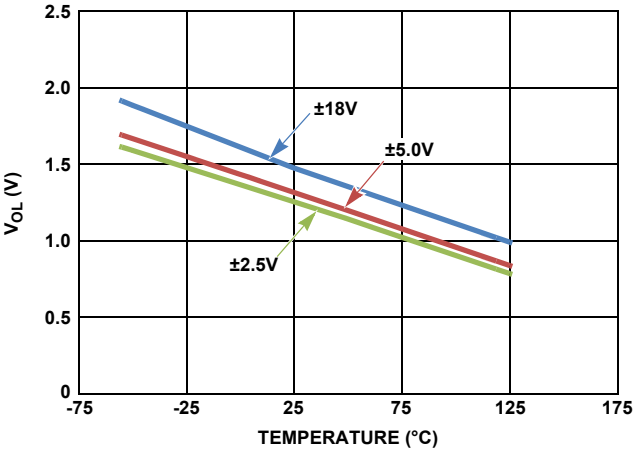


FIGURE 19. V_{OL} vs TEMPERATURE (R_L = 2k)

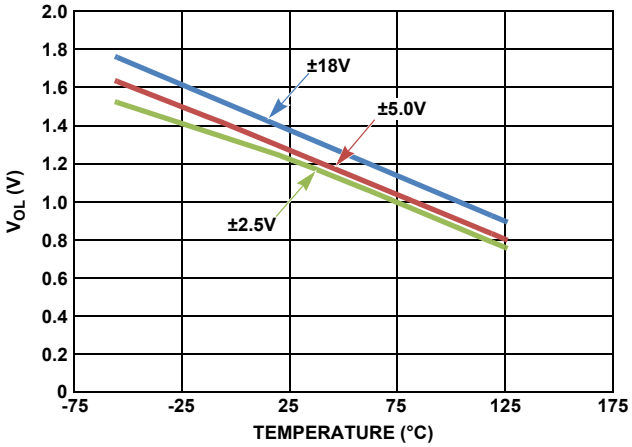


FIGURE 20. V_{OL} vs TEMPERATURE (R_L = 5k)

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

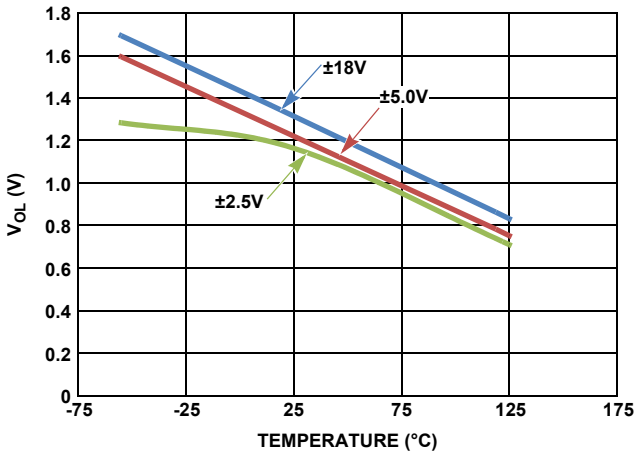


FIGURE 21. V_{OL} vs TEMPERATURE (R_L = 10k)

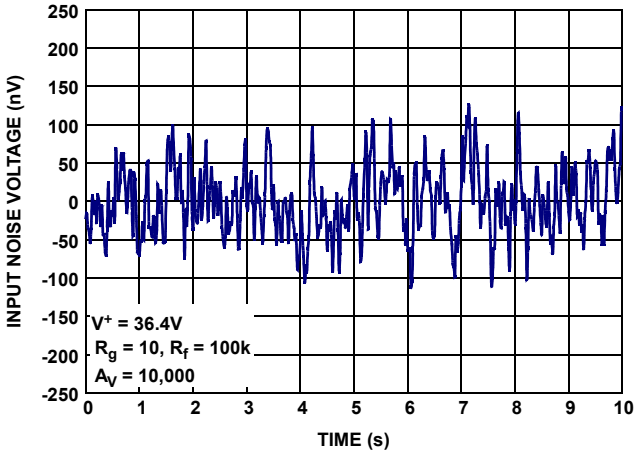


FIGURE 22. INPUT NOISE VOLTAGE (0.1Hz TO 10Hz)

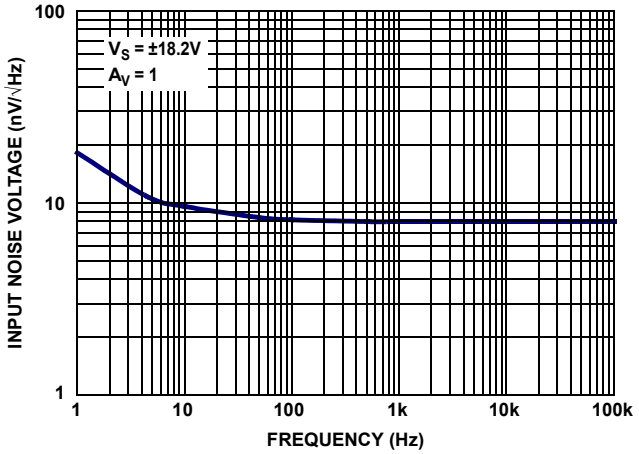


FIGURE 23. INPUT NOISE VOLTAGE SPECTRAL DENSITY

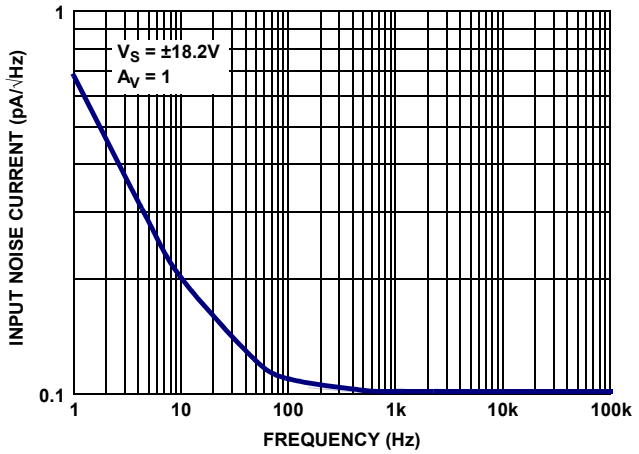


FIGURE 24. INPUT NOISE CURRENT SPECTRAL DENSITY

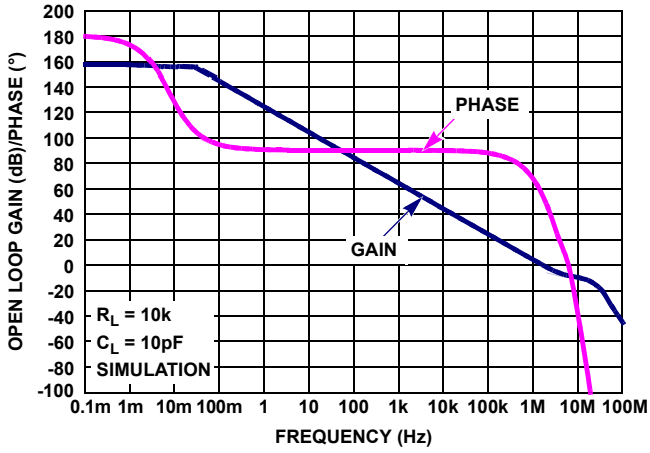


FIGURE 25. OPEN-LOOP GAIN, PHASE vs FREQUENCY (R_L = 10kΩ, C_L = 10pF)

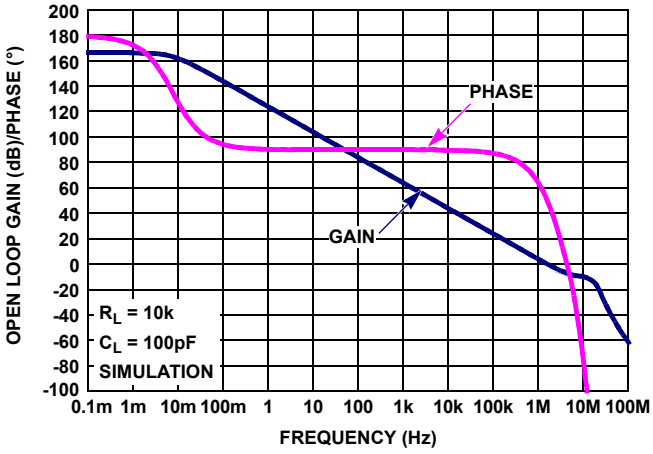


FIGURE 26. OPEN LOOP FREQUENCY RESPONSE (R_L = 10kΩ, C_L = 100pF)

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

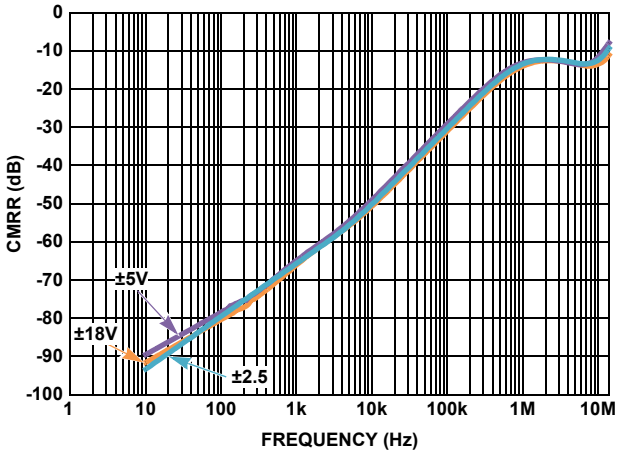


FIGURE 27. CMRR vs SUPPLY VOLTAGE (+25°C)

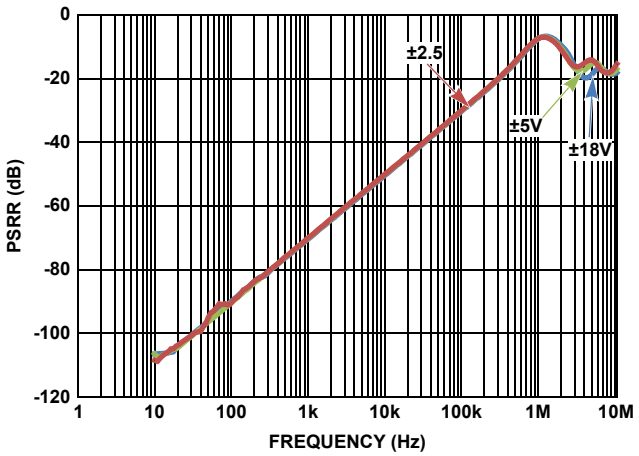


FIGURE 28. PSRR vs SUPPLY VOLTAGE (+25°C)

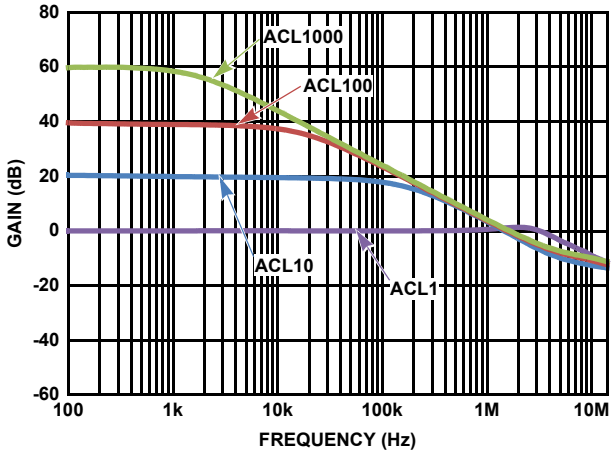


FIGURE 29. FREQUENCY RESPONSE vs ACL (±2.5V)

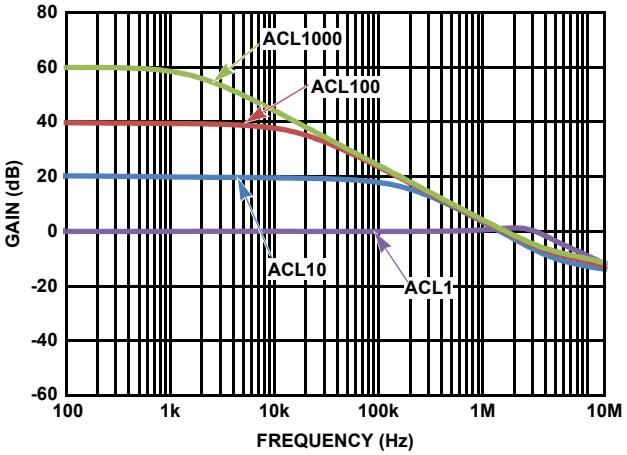


FIGURE 30. FREQUENCY RESPONSE vs ACL (±5.0V)

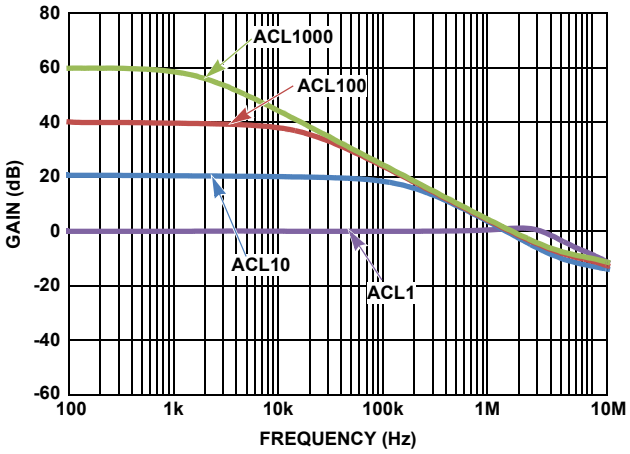


FIGURE 31. FREQUENCY RESPONSE vs ACL (±18.0V)

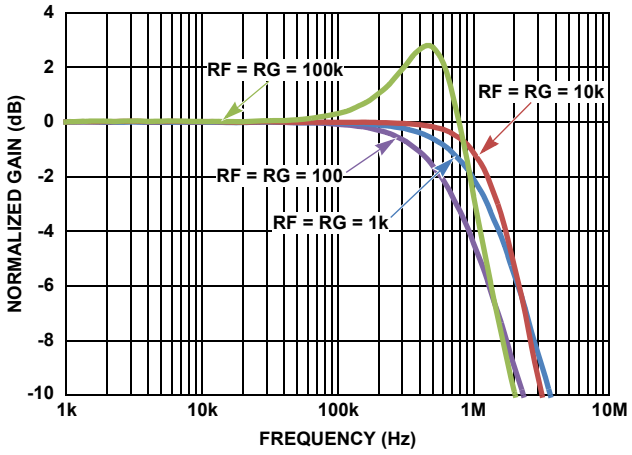


FIGURE 32. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE (±2.5V)

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

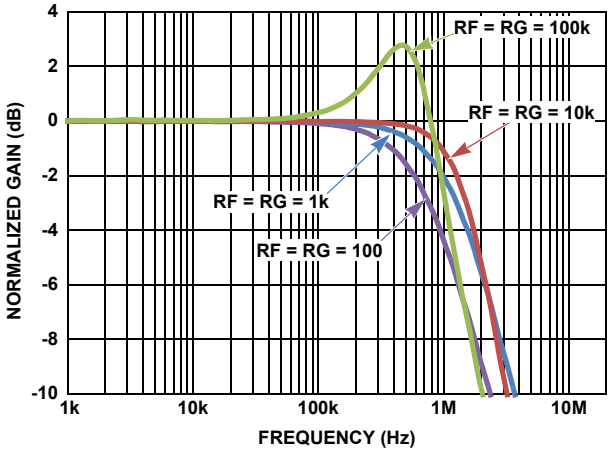


FIGURE 33. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE (±5.0V)

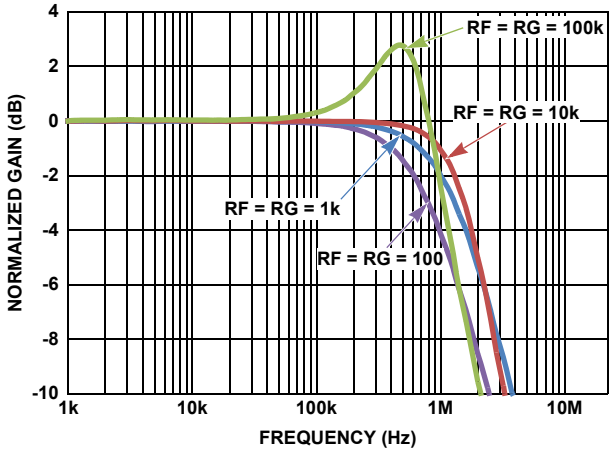


FIGURE 34. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE (±18.0V)

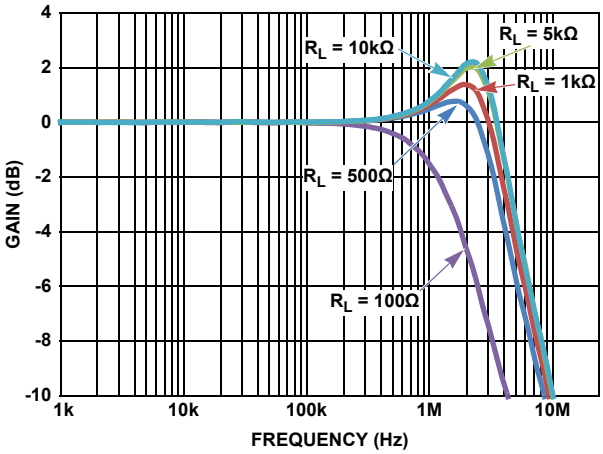


FIGURE 35. FREQUENCY RESPONSE vs R_L (±2.5V)

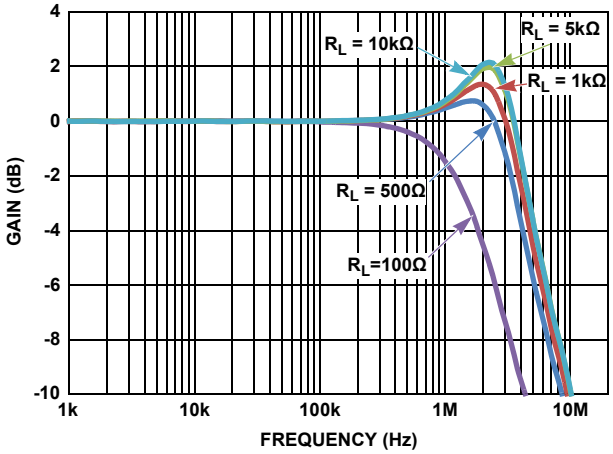


FIGURE 36. FREQUENCY RESPONSE vs R_L (±5.0V)

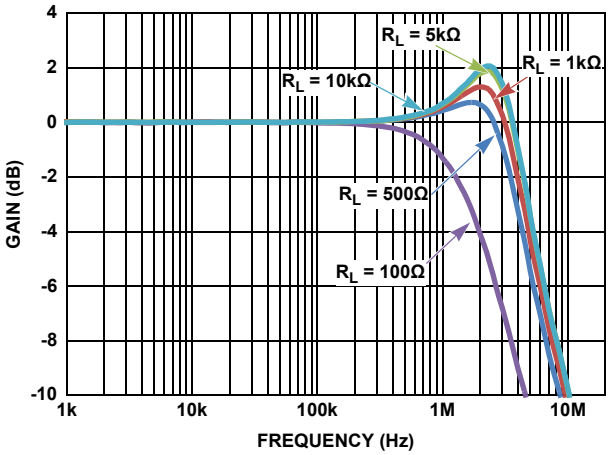


FIGURE 37. FREQUENCY RESPONSE vs R_L (±18.0V)

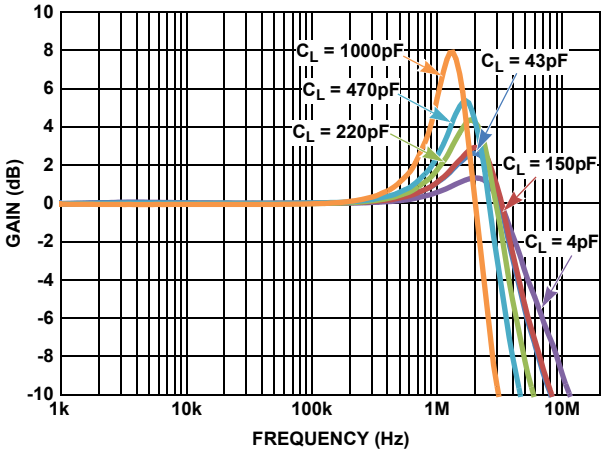


FIGURE 38. FREQUENCY RESPONSE vs C_L (±2.5V)

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

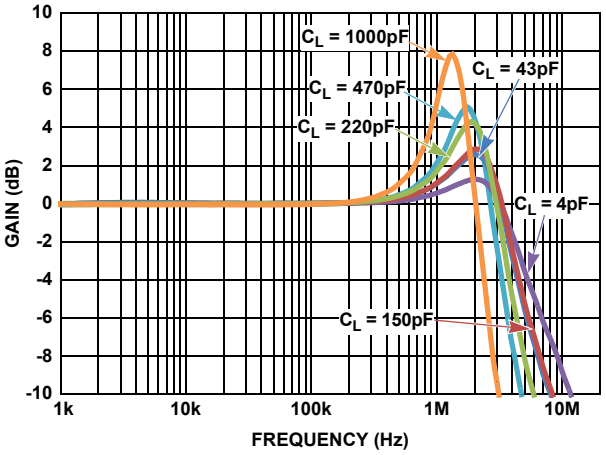


FIGURE 39. FREQUENCY RESPONSE vs C_L (±5.0V)

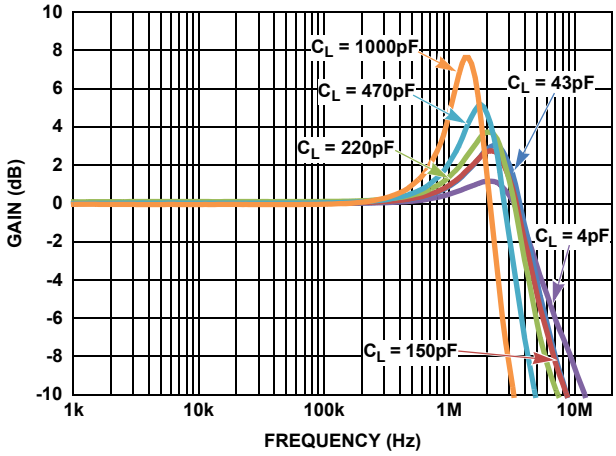


FIGURE 40. FREQUENCY RESPONSE vs C_L (±18.0V)

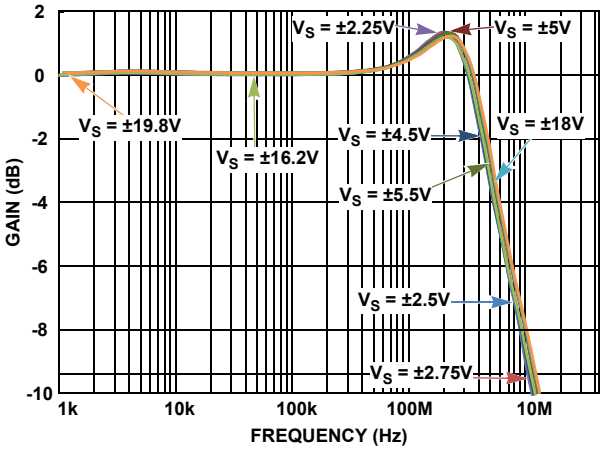


FIGURE 41. FREQUENCY RESPONSE vs SUPPLY VOLTAGE (+25°C)

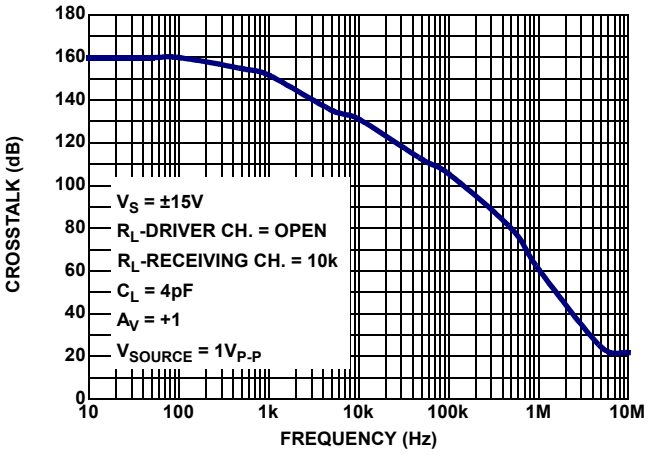


FIGURE 42. CROSSTALK (+25°C)

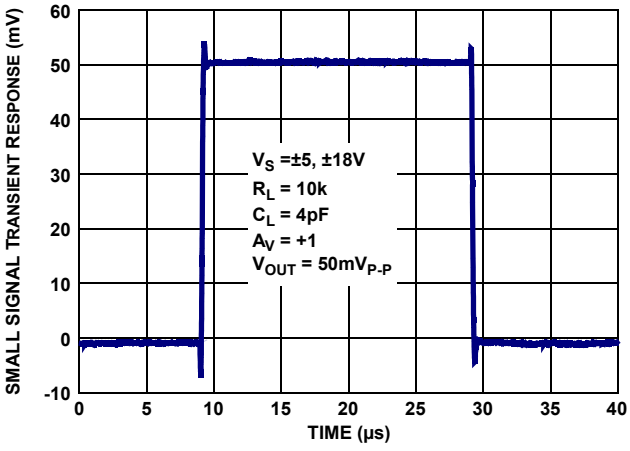


FIGURE 43. SMALL SIGNAL TRANSIENT RESPONSE (+25°C)

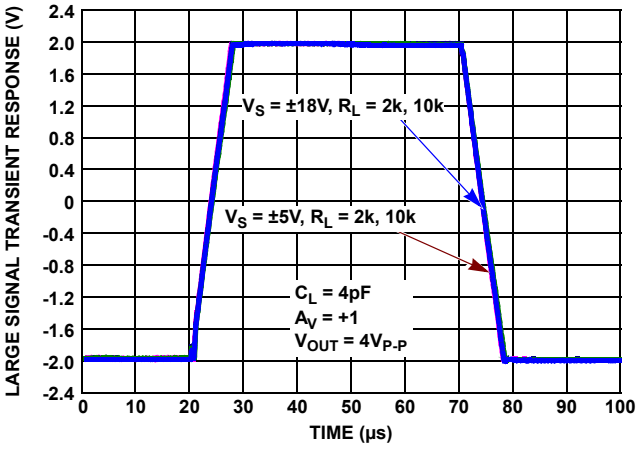


FIGURE 44. LARGE SIGNAL TRANSIENT RESPONSE (+25°C)

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

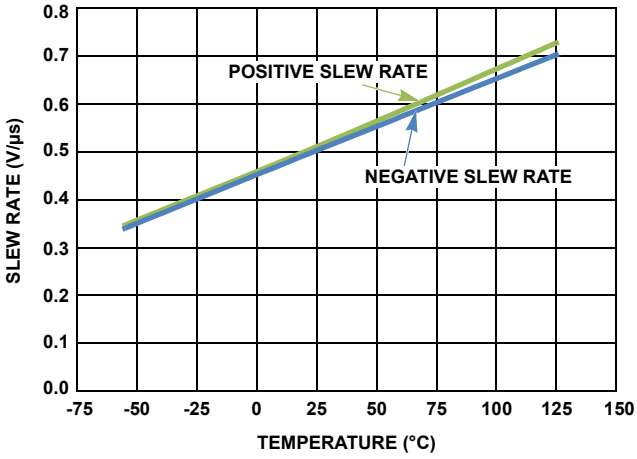


FIGURE 45. SLEW RATE vs TEMPERATURE V_S = ±2.5

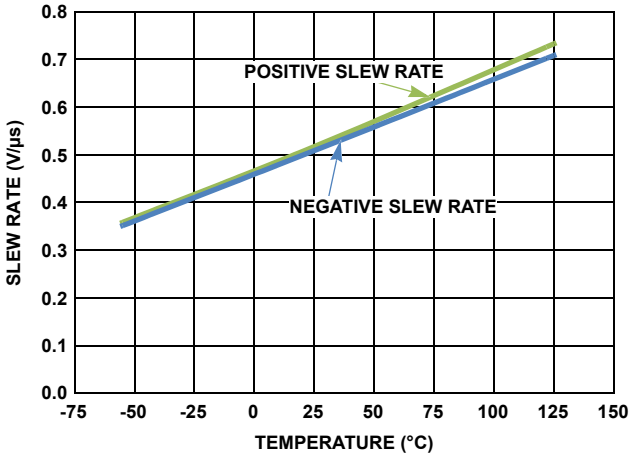


FIGURE 46. SLEW RATE vs TEMPERATURE V_S = ±5V

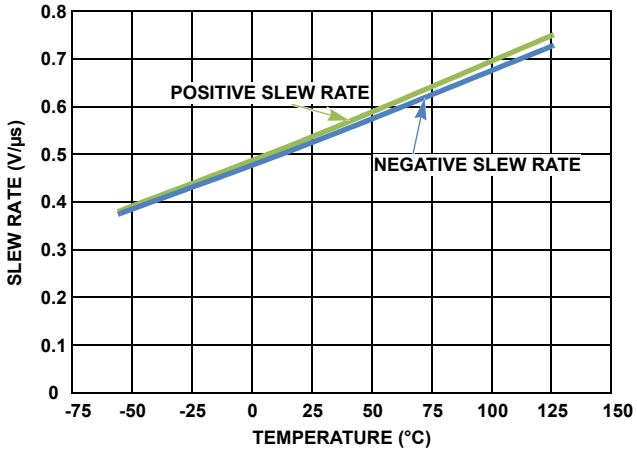


FIGURE 47. SLEW RATE vs TEMPERATURE V_S = ±18V

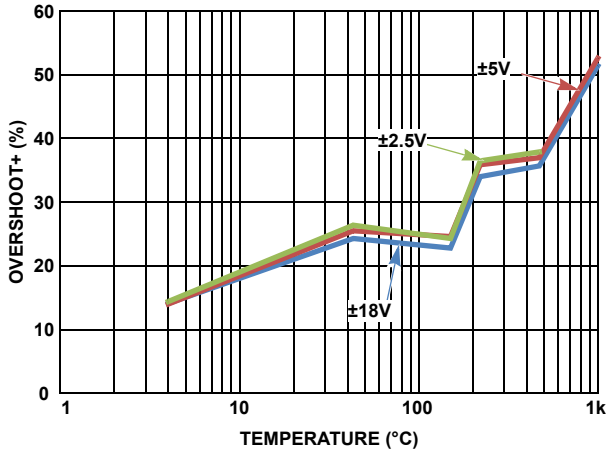


FIGURE 48. OVERSHOOT + vs CAPACITANCE

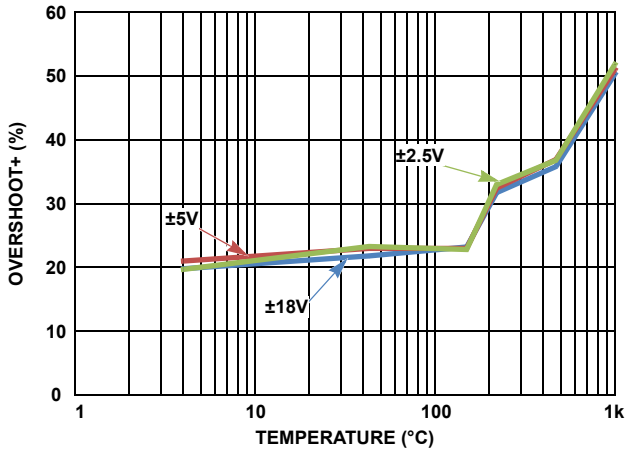


FIGURE 49. OVERSHOOT - vs CAPACITANCE

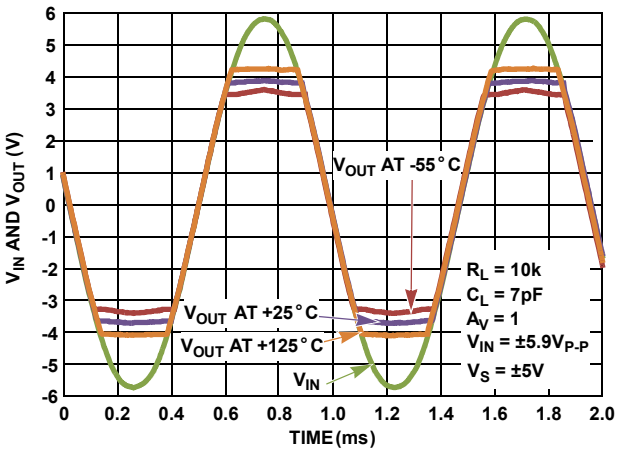


FIGURE 50. OUTPUT OVERDRIVE RESPONSE vs TEMPERATURE

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

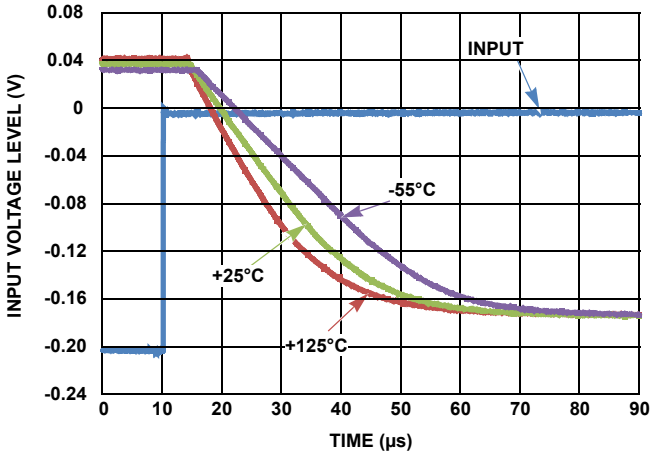


FIGURE 51. ±18V POSITIVE SATURATION RECOVERY TIME (+25°C)

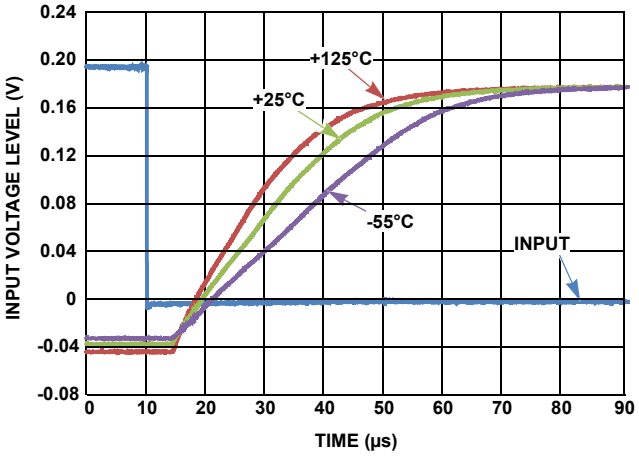


FIGURE 52. ±18V NEGATIVE SATURATION RECOVERY TIME (+25°C)

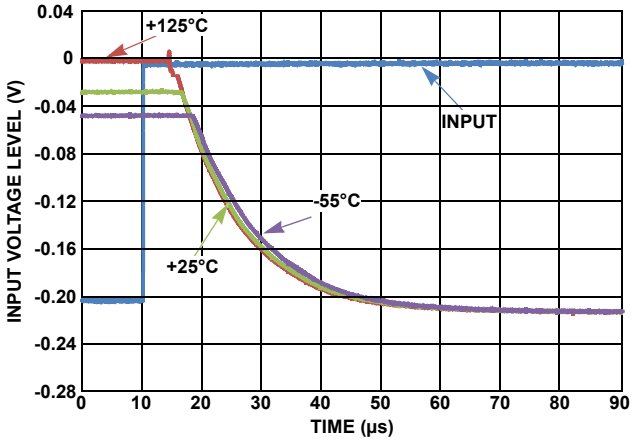


FIGURE 53. ±5V POSITIVE SATURATION RECOVERY TIME (+25°C)

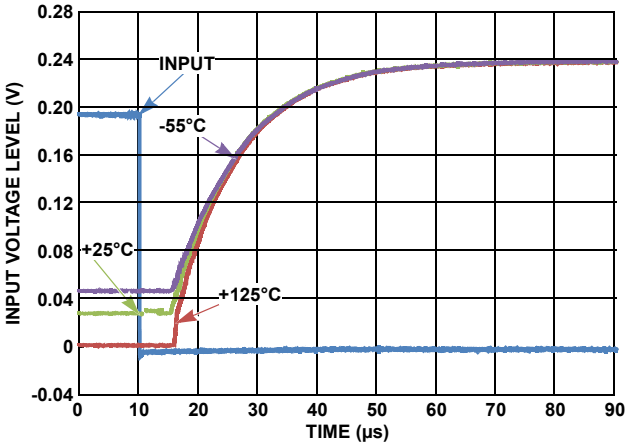


FIGURE 54. ±5V NEGATIVE SATURATION RECOVERY TIME (+25°C)

Post High Dose Rate Radiation Characteristics

Unless otherwise specified, V_S ± 19.8V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

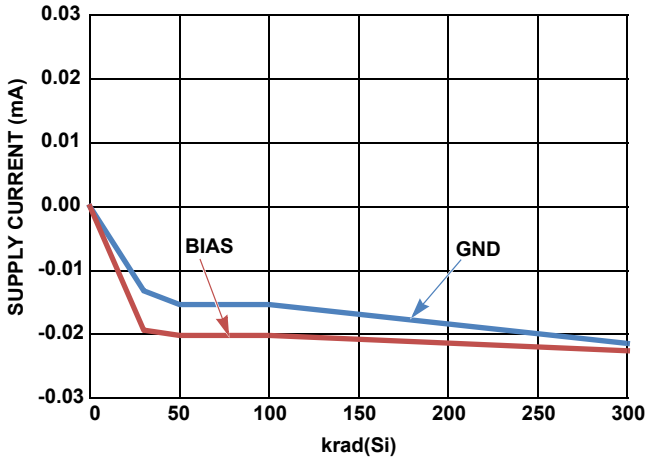


FIGURE 55. SUPPLY CURRENT SHIFT vs HDR RADIATION

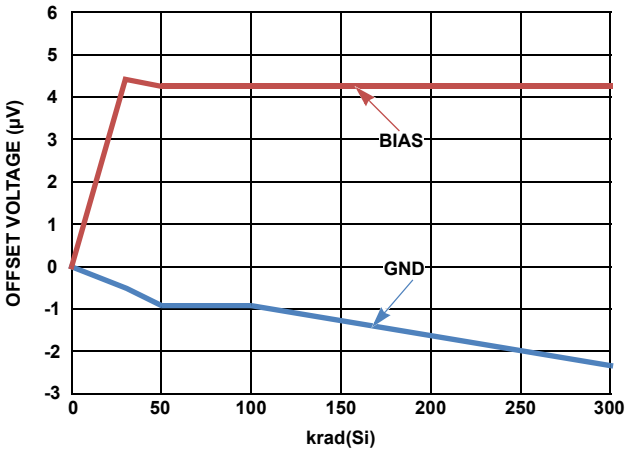


FIGURE 56. OFFSET VOLTAGE SHIFT vs HDR RADIATION

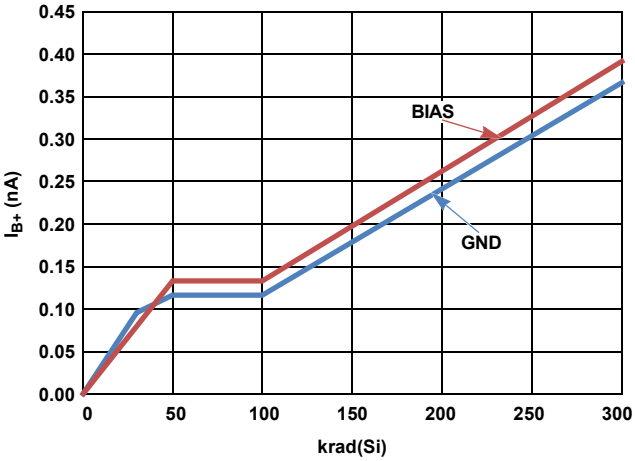


FIGURE 57. POSITIVE INPUT BIAS CURRENT SHIFT vs HDR RADIATION

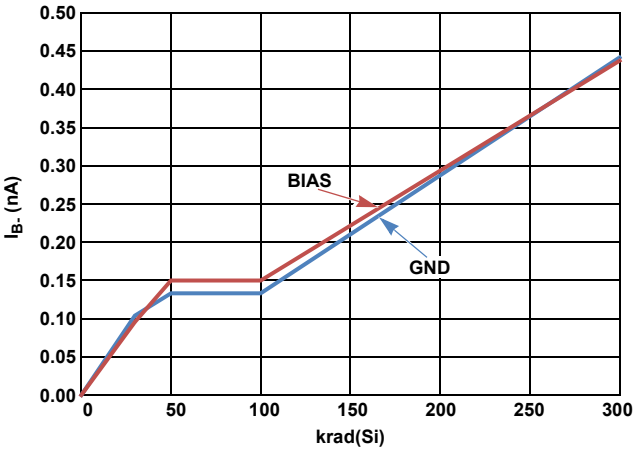


FIGURE 58. NEGATIVE INPUT BIAS CURRENT SHIFT vs HDR RADIATION

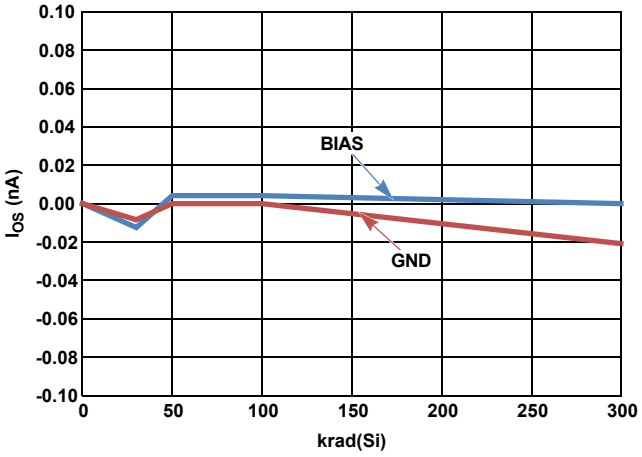


FIGURE 59. INPUT OFFSET CURRENT SHIFT vs HDR RADIATION

Post Low Dose Rate Radiation Characteristics

Unless otherwise specified, V_S ± 19.8V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

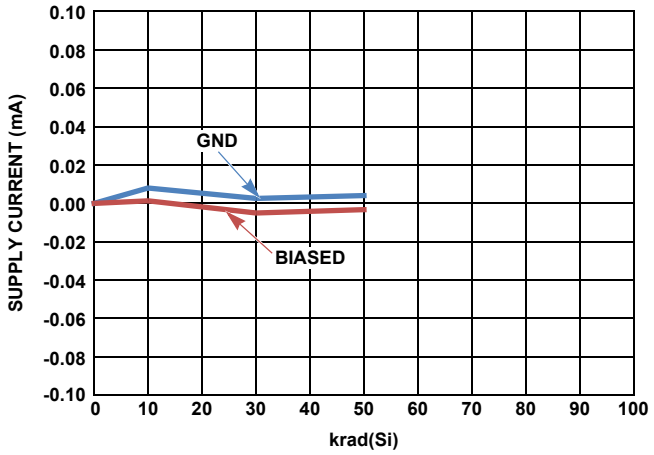


FIGURE 60. SUPPLY CURRENT SHIFT vs LDR RADIATION

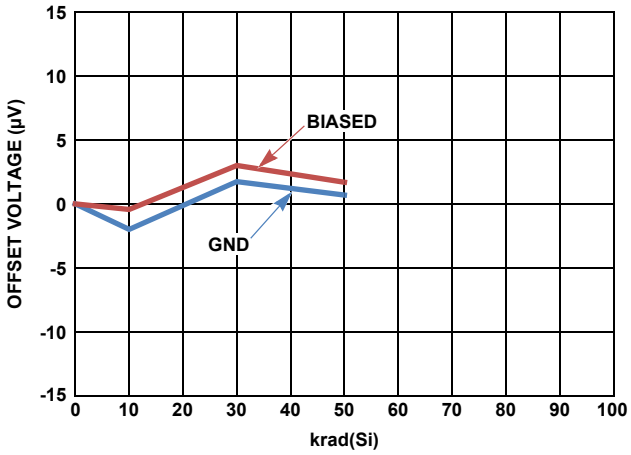


FIGURE 61. OFFSET VOLTAGE SHIFT vs LDR RADIATION

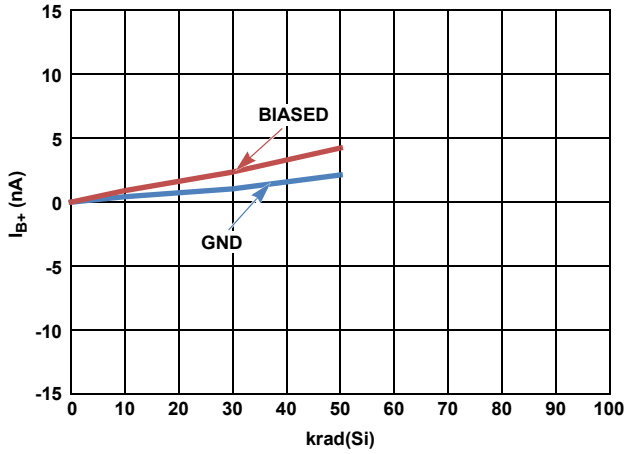


FIGURE 62. POSITIVE INPUT BIAS CURRENT SHIFT vs LDR RADIATION

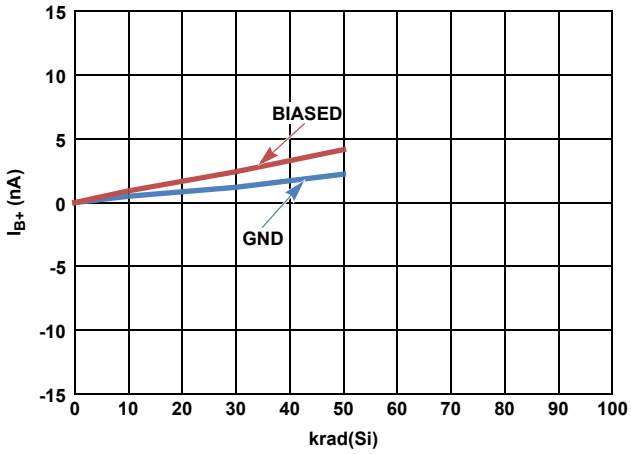


FIGURE 63. NEGATIVE INPUT BIAS CURRENT SHIFT vs LDR RADIATION

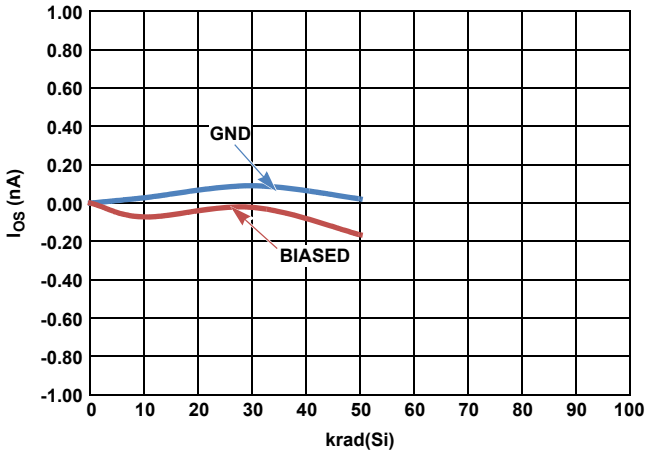


FIGURE 64. INPUT OFFSET CURRENT SHIFT vs LDR RADIATION

Applications Information

Functional Description

The ISL70219ASEH and ISL70419ASEH are dual and quad, low noise precision op amps. These devices are fabricated in a new precision 40V complementary bipolar DI process. A super-beta NPN input stage with input bias current cancellation provides low input bias current (180pA typical), low input offset voltage (13µV typical), low input noise voltage (8nV/√Hz), and low 1/f noise corner frequency (~8Hz). These amplifiers also feature high open loop gain (14kV/mV) for excellent CMRR (145dB) and THD+N performance (0.0005% at $3.5V_{RMS}$, 1kHz into 2kΩ). A complementary bipolar output stage enables high capacitive load drive without external compensation.

Operating Voltage Range

The devices are designed to operate across the 4.5V (±2.25V) to 40V (±20V) voltage range and are fully characterized at 10V (±5V) and 36V (±18V). The Power Supply Rejection Ratio typically exceeds 140dB across the full operating voltage range and 120dB minimum across the -55°C to +125°C temperature range. The worst case common mode input voltage range over-temperature is 2V to each rail. With ±18V supplies, CMRR performance is typically >130dB over-temperature. The minimum CMRR performance across the -55°C to +125°C temperature range is >120dB for power supply voltages from ±5V (10V) to ±18V (36V).

Input Performance

The super-beta NPN input pair provides excellent frequency response while maintaining high input precision. High NPN beta (>1000) reduces input bias current while maintaining good frequency response, low input bias current and low noise. Input bias cancellation circuits provide additional bias current reduction to <5nA, and excellent temperature stabilization. Figures 6 through 8 show the high degree of bias current stability at ±5V and ±18V supplies that is maintained across the -55°C to +125°C temperature range. The low bias current TC also produces very low input offset current TC, which reduces DC input offset errors in precision, high impedance amplifiers.

The +25°C maximum input offset voltage (V_{OS}) is 85µV at ±18V supplies. Input offset voltage temperature coefficients ($V_{OS}TC$) is a maximum of ±1.0µV/°C. The V_{OS} temperature behavior is smooth (Figures 3 through 5) maintaining constant TC across the entire temperature range.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 500Ω current limiting resistors and an antiparallel diode pair across the inputs (Figure 65).

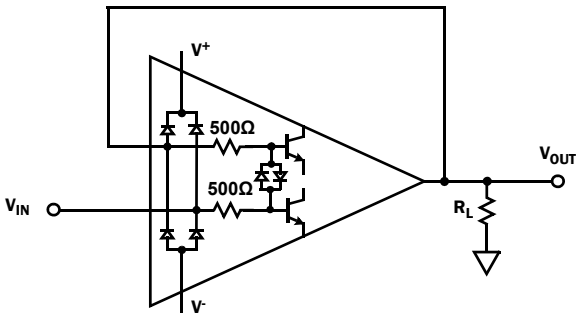


FIGURE 65. INPUT ESD DIODE CURRENT LIMITING - UNITY GAIN

The series resistors limit the high feed-through currents that can occur in pulse applications when the input dV/dt exceeds the 0.5V/µs slew rate of the amplifier. Without the series resistors, the input can forward-bias the antiparallel diodes causing current to flow to the output resulting in severe distortion and possible diode failure.

Figure 36 provides an example of distortion free large signal response using a $4V_{P-P}$ input pulse with an input rise time of <1ns. The series resistors enable the input differential voltage to be equal to the maximum power supply voltage (40V) without damage.

In applications where one or both amplifier input terminals are at risk of exposure to high voltages beyond the power supply rails, current limiting resistors may be needed at the input terminal to limit the current through the power supply ESD diodes to 20mA maximum.

Output Current Limiting

The output current is internally limited to approximately ±45mA at +25°C and can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only 1 amplifier at a time for the dual/quad op amp. Continuous operation under these conditions may degrade long term reliability. Figure 14 shows the current limit variation with temperature.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL70219ASEH and ISL70419ASEH are immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

ISL70219ASEH

Die Characteristics

Die Dimensions

2406µm x 2935µm (95mils x 116mils)
Thickness: 483µm ± 25µm (19mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Nitride/Silicon Dioxide Sandwich
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

PROCESS

PR40 (DI)

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

ADDITIONAL INFORMATION

WORST CASE CURRENT DENSITY

$< 2 \times 10^5$ A/cm^2

TRANSISTOR COUNT

466

Weight of Packaged Device

0.3958 grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Unbiased, tied to package pin 6
Case Isolation to Any Lead: $20 \times 10^9\Omega$ (min)

Metallization Mask Layout

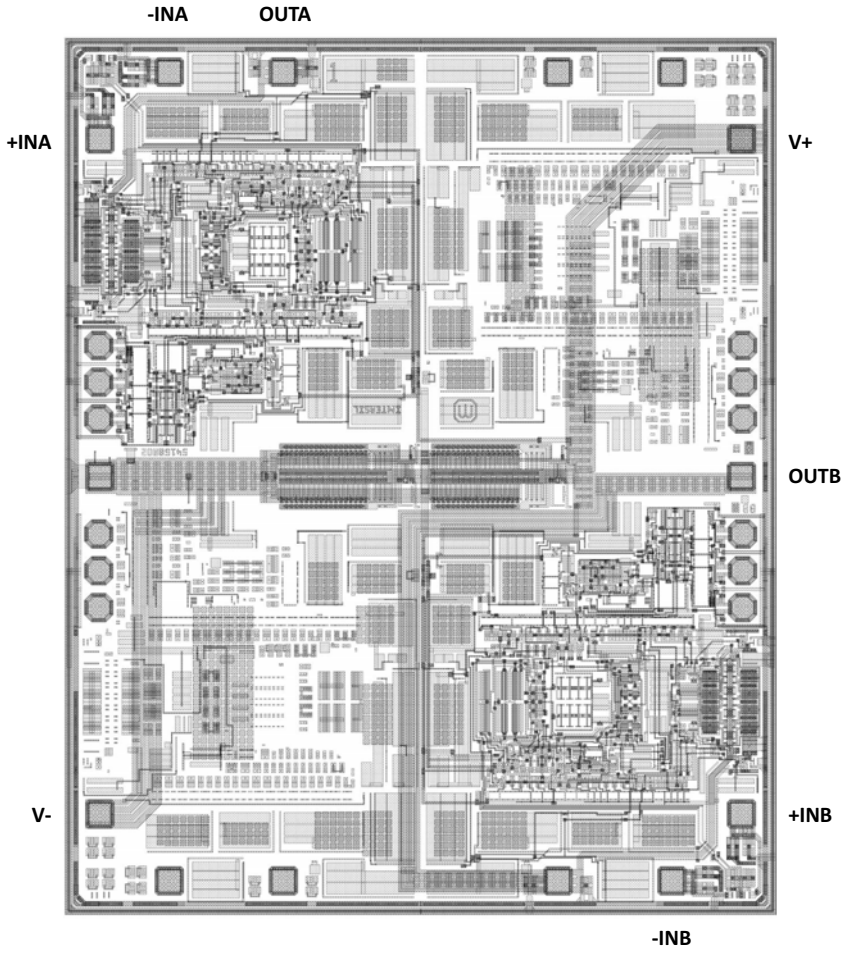


TABLE 1. ISL70219ASEH DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES PER PAD
OUTB	1	2195.0	1418.0	70	70	1
V^+	2	2195.0	2510.0	70	70	1
OUTA	3	709.0	2727.0	70	70	1
-INA	4	339.0	2727.0	70	70	1
+INA	5	114.0	2510.0	70	70	1
V^-	6	114.0	336.0	70	70	1
+INB	7	2195.0	336.0	70	70	1
-INB	8	1970.0	110.0	70	70	1

NOTE:

8. Origin of coordinates is the bottom left corner of the die.

ISL70419ASEH

Die Characteristics

Die Dimensions

2406µm x 2935µm (95mils x 116mils)
Thickness: 483µm ± 25µm (19mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Nitride/Silicon Dioxide Sandwich
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

PROCESS

PR40 (DI)

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

ADDITIONAL INFORMATION

WORST CASE CURRENT DENSITY

$< 2 \times 10^5$ A/cm^2

TRANSISTOR COUNT

482

Weight of Packaged Device

0. 6043 grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Unbiased, tied to package E-pad
Case Isolation to Any Lead: 20×10^9 Ω (min)

Metallization Mask Layout

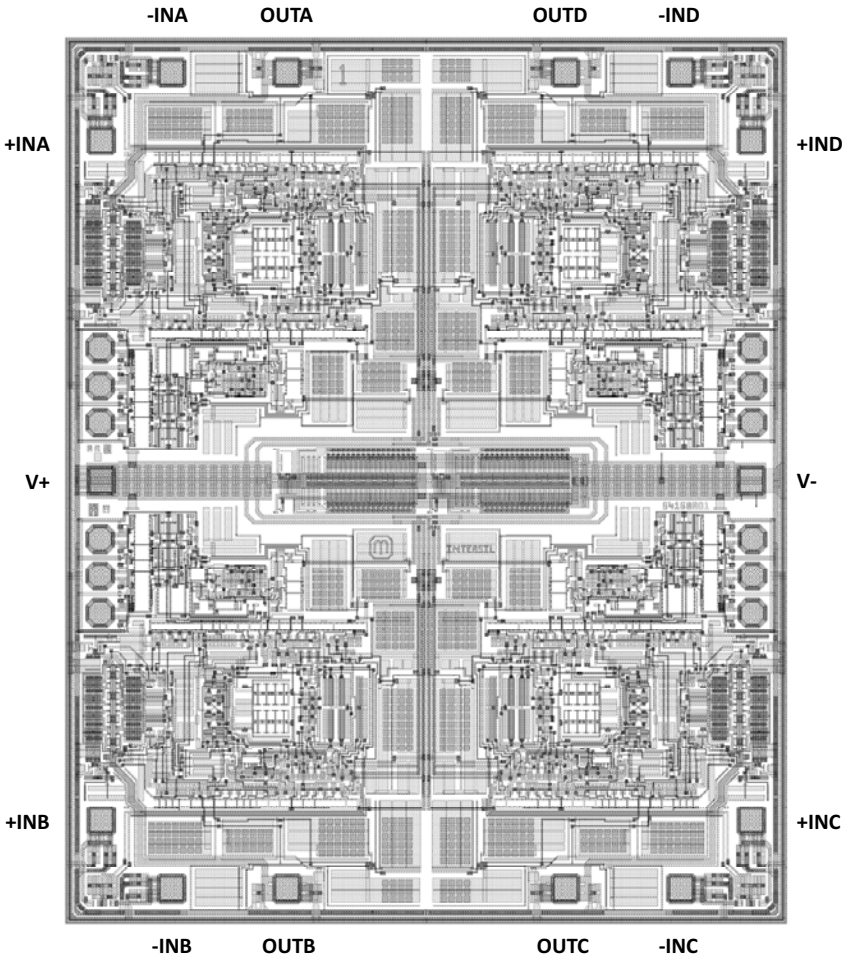


TABLE 2. ISL70419ASEH DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES PER PAD
OUTA	3	709.0	2727.0	70	70	1
-INA	4	339.0	2727.0	70	70	1
+INA	5	114.0	2501.0	70	70	1
V^+	9	114.0	1419.0	70	70	1
-INB	13	339.0	110.0	70	70	1
+INB	14	114.0	327.0	70	70	1
OUTB	15	709.0	110.0	70	70	1
OUTC	16	1600.0	110.0	70	70	1
-INC	17	1970.0	110.0	70	70	1
+INC	18	2195.0	327.0	70	70	1
V^-	22	2195.0	1419.0	70	70	1
-IND	26	1970.0	2727.0	70	70	1
+IND	1	2195.0	2501.0	70	70	1
OUTD	2	1600.0	2727.0	70	70	1

NOTE:

9. Origin of coordinates is the bottom left corner of die.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 27, 2014	FN8459.0	Initial Release.

About Intersil

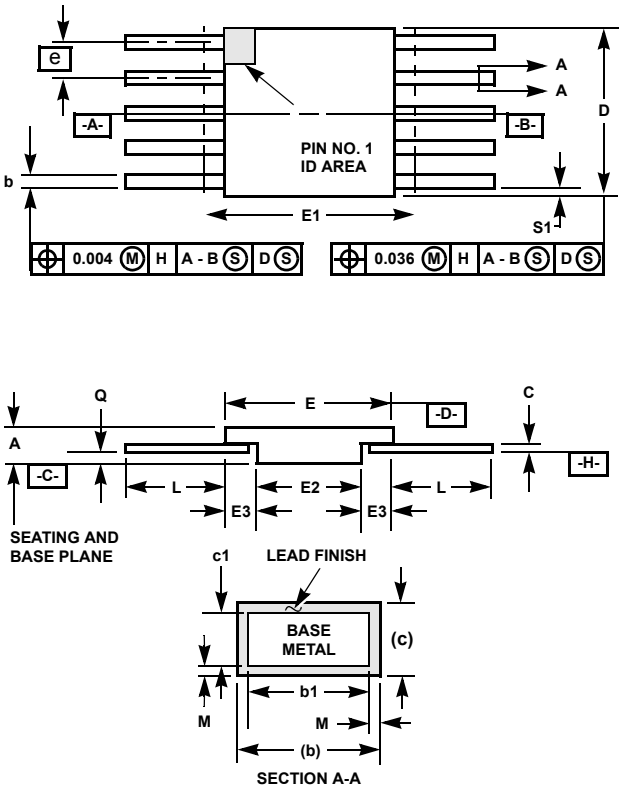
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

Ceramic Metal Seal Flatpack Packages (Flatpack)



K10.A MIL-STD-1835 CDFP3-F10 (F-4A, CONFIGURATION B)
10 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.290	-	7.37	3
E	0.240	0.260	6.10	6.60	-
E1	-	0.280	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	10		10		-

Rev. 0 3/07

NOTES:

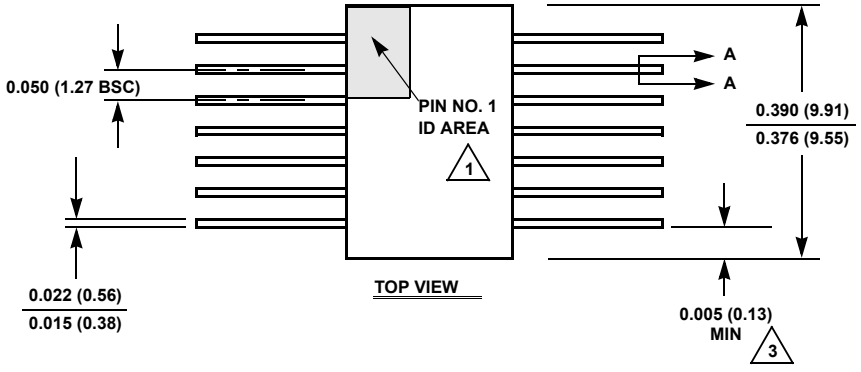
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

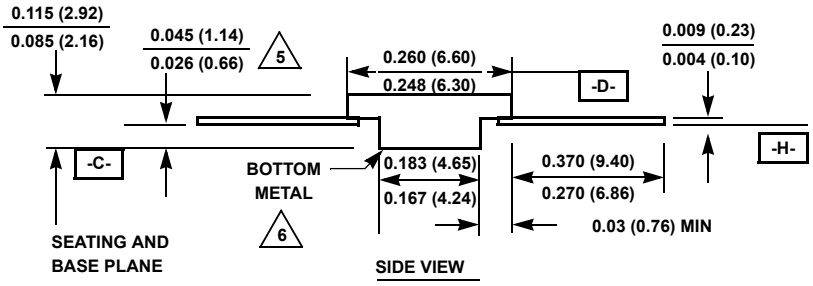
Package Outline Drawing

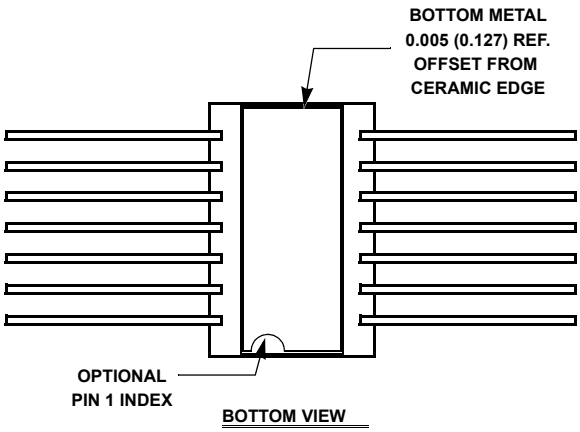
K14.C

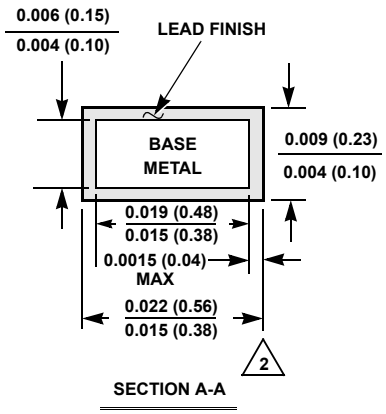
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 0, 9/12









NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Measure dimension at all four corners.
4. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
5. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
6. The bottom of the package is a solderable metal surface.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Dimensions: INCH (mm). Controlling dimension: INCH.